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An embedded system is a computer system—a combination of a computer processor, computer memory, and input/output peripheral devices—that has a dedicated function within a larger mechanical or electrical system. It is embedded as part of a complete device often including electrical or electronic hardware and mechanical parts. Because an embedded system typically controls physical operations ...

Ranging from low-level application and architecture optimizations to high-level modeling and exploration concerns, this authoritative reference compiles essential research on various levels of abstraction appearing in embedded systems and software design. It promotes platform-based design for improved system implementation and modeling and enhanced

This book constitutes the refereed proceedings of the 8th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2008, held in Samos, Greece, in July 2008. The 24 revised full papers presented together with a contemplative keynote and additional papers of two special workshop sessions were carefully reviewed and selected from 62 submissions. The papers are organized in topical sections on architecture, new frontiers, SoC, application specific contributions, system level design for heterogeneous systems, programming multicores, sensors and sensor networks; and systems modeling and design.

This book constitutes the refereed proceedings of the 4th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2004, held in Samos, Greece on July 2004. Besides the SAMOS 2004 proceedings, the book also presents 19 revised papers from the predecessor workshop SAMOS 2003. The 55 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in topical sections on reconfigurable computing, architectures and implementation, and systems modeling and simulation.

The SAMOS workshop is an international gathering of highly qualified researchers from academia and industry, sharing in a 3-day lively discussion on the quiet and - spiring northern mountainside of the Mediterranean island of Samos. As a tradition, the workshop features workshop presentations in the morning, while after lunch all kinds of informal discussions and nut-cracking gatherings take place. The workshop is unique in the sense that not only solved research problems are presented and discussed but also (partly) unsolved problems and in-depth topical reviews can be unleashed in the sci-ti?c arena. Consequently, the workshop provides the participants with an environment where collaboration rather than competition is fostered. The earlier workshops, SAMOS I-IV (2001-2004), were composed only of invited presentations. Due to increasing expressions of interest in the workshop, the Program Committee of SAMOS V decided to open the workshop for all submissions. As a result the SAMOS workshop gained an immediate popularity; a total of 114 submitted papers were received for evaluation. The papers came from 24 countries and regions: Austria (1), Belgium (2), Brazil (5), Canada (4), China (12), Cyprus (2), Czech

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Republic (1), Finland (15), France (6), Germany (8), Greece (5), Hong Kong (2), India (2), Iran (1), Korea (24), The Netherlands (7), Pakistan (1), Poland (2), Spain (2), Sweden (2), T- wan (1), Turkey (2), UK (2), and USA (5). We are grateful to all of the authors who submitted papers to the workshop.

Three approaches can be applied to determine the performance of parallel and distributed computer systems: measurement, simulation, and mathematical methods. This book introduces various network architectures for parallel and distributed systems as well as for systems-on-chips, and presents a strategy for developing a generator for automatic model derivation. It will appeal to researchers and students in network architecture design and performance analysis.

After nearly six years as the field's leading reference, the second edition of this award-winning handbook reemerges with completely updated content and a brand new format. The Computer Engineering Handbook, Second Edition is now offered as a set of two carefully focused books that together encompass all aspects of the field. In addition to complete updates throughout the book to reflect the latest issues in low-power design, embedded processors, and new standards, this edition includes a new section on computer memory and storage as well as several new chapters on such topics as semiconductor memory circuits, stream and wireless processors, and nonvolatile memory technologies and applications.

New design architectures in computer systems have surpassed industry expectations. Limits, which were once thought of as fundamental, have now been broken. Digital Systems and Applications details these innovations in systems design as well as cutting-edge applications that are emerging to take advantage of the fields increasingly sophisticated capabilities. This book features new chapters on parallelizing iterative heuristics, stream and wireless processors, and lightweight embedded systems. This fundamental text— Provides a clear focus on computer systems, architecture, and applications Takes a top-level view of system organization before moving on to architectural and organizational concepts such as superscalar and vector processor, VLIW architecture, as well as new trends in multithreading and multiprocessing. includes an entire section dedicated to embedded systems and their applications Discusses topics such as digital signal processing applications, circuit implementation aspects, parallel I/O algorithms, and operating systems Concludes with a look at new and future directions in computing Features articles that describe diverse aspects of computer usage and potentials for use Details implementation and performance-enhancing techniques such as branch prediction, register renaming, and virtual memory Includes a section on new directions in computing and their penetration into many new fields and aspects of our daily lives

Satisfiability (SAT) related topics have attracted researchers from various disciplines: logic, applied areas such as planning, scheduling, operations research and combinatorial optimization, but also theoretical issues on the theme of complexity and much more, they all are connected through SAT. My personal interest in SAT stems from actual solving: The increase in power of modern SAT solvers over the past 15 years has been phenomenal. It has become the key enabling technology in automated verification of both computer hardware and software. Bounded Model Checking (BMC) of computer hardware is now probably the most widely used model checking technique. The counterexamples that it finds are just satisfying instances of a Boolean formula obtained by unwinding to some fixed depth a sequential circuit and its specification in linear temporal logic. Extending model checking to software verification is a much more difficult problem on the frontier of current research. One promising approach for languages like C with finite word-length integers is to use the same idea as in BMC but with a decision procedure for the theory of bit-vectors instead of SAT. All decision procedures for bit-vectors that I am familiar with ultimately make use of a fast SAT solver to handle complex formulas. Decision procedures for more complicated theories, like linear real and integer arithmetic, are also used in program verification. Most of them use powerful SAT solvers in an essential way. Clearly, efficient SAT solving is a key technology for 21st century computer science. I expect this collection of papers on all theoretical and practical aspects of SAT solving will be extremely useful to both students and researchers and will lead to many further advances in the field.' Edmund Clarke (FORE Systems University Professor of Computer Science and Professor of Electrical and Computer Engineering at Carnegie Mellon University)

The past few years have seen significant change in the landscape of high-end network processing. In response to the formidable challenges facing this emerging field, the editors of this series set out to survey the latest research and practices in the design, programming, and use of network processors. Through chapters on hardware, software, performance and modeling, Network Processor Design illustrates the potential for new NP applications, helping to lay a theoretical foundation for the architecture, evaluation, and programming of networking processors. Like Volume 2 of the series, Volume 3 further shifts the focus from achieving higher levels of packet processing performance to addressing other critical factors such as ease of programming, application developments, power, and performance prediction. In addition, Volume 3 emphasizes forward-looking, leading-edge research in the areas of architecture, tools and techniques, and applications such as high-speed intrusion detection and prevention system design, and the implementation of new interconnect standards. Investigates current applications of network processor technology at Intel; Infineon Technologies; and NetModule Presents current research in network processor design in three distinct areas: Architecture at Washington University, St. Louis; Oregon Health and Science University; University of Georgia; and North Carolina State University. Tools and Techniques at University of Texas, Austin; Academy of Sciences, China; University of Paderborn, Germany; and University of Massachusetts, Amherst. Applications at University of California, Berkeley; Universidad Complutense de Madrid, Spain; ETH Zurich, Switzerland; Georgia Institute of Technology; Vrije Universiteit, the Netherlands; and Universiteit Leiden, the Netherlands.

Network on Chip (NoC) addresses the communication requirement of different nodes on System on Chip. The

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bio-inspired algorithms improve the bandwidth utilization, maximize the throughput and reduce the end-to-end latency and inter-flit arrival time. This book exclusively presents in-depth information regarding bio-inspired algorithms solving real world problems focussing on fault-tolerant algorithms inspired by the biological brain and implemented on NoC. It further documents the bio-inspired algorithms in general and more specifically, in the design of NoC. It gives an exhaustive review and analysis of the NoC architectures developed during the last decade according to various parameters. Key Features: Covers bio-inspired solutions pertaining to Network-on-Chip (NoC) design solving real world examples Includes bio-inspired NoC fault-tolerant algorithms with detail coding examples Lists fault-tolerant algorithms with detailed examples Reviews basic concepts of NoC Discusses NoC architectures developed-to-date

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